UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/599,901	04/19/2007	Georg Busch	112740-1145	6294

29177 7590 10/06/2008

BELL, BOYD & LLOYD, LLP
P.O. BOX 1135
CHICAGO, IL 60690

EXAMINER	
CAZAN, LIVIUS RADU	
ART UNIT	PAPER NUMBER
3729	
MAIL DATE	DELIVERY MODE
10/06/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/599,901	BUSCH, GEORG	
	Examiner	Art Unit	
	LIVIUS R. CAZAN	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/6/2008 has been entered.

Claim Rejections - 35 USC § 102

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. **Claims 6, 8, 13, 15, 20, and 22** are rejected under 35 U.S.C. 102(b) as being anticipated by Hirose (US6407345).

4. **Regarding claims 6, 13, and 20**, Hirose discloses drilling through-holes (36, Fig. 1B) in a substrate and performing electroless plating to plate the inside of the holes and the substrate (see step (1) in col. 15), etching a strip conductor image into the plated layer (34, Fig. 1C; see step (1) in col. 15), filling the holes with a medium (40, Figs. 2E-2G; see step (4) in col. 15), lacquering the surfaces of the substrate (see Fig. 2H; see step (8) in col. 16) and applying an insulating lacquer (44, 46, 50, Fig. 2H) to the surfaces of the circuit board, and producing strip conductors (54, Figs. 4N and 4O; see steps (13) and (14) in col. 17) arranged above the through-connections. Hirose does not mention any brushing of the circuit board during the step of lacquering, and no other

layers are formed between the steps of etching and applying an insulating lacquer. See ln. 67 in col. 15 to ln. 5 of col. 16. See *Response to Arguments* below.

5. **Regarding claims 8, 15, and 22**, the lacquer is inherently non-resistant to etching, since there must exist some sort of etching process which will etch the lacquer, be it a chemical etching process or a physical etching process.

Claim Rejections - 35 USC § 103

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. **Claims 7, 11, 14, 18, 21, and 25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose.

8. **Regarding claims 7, 14, and 21**, Hirose discloses substantially the same invention as the Applicant, except for the medium used to fill the holes and the insulating lacquer being identical.

9. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to choose a medium and a lacquer suitable for the intended use, since this requires only routine skill in the art. As such, it would have been obvious for one of ordinary skill in the art to utilize the same material for the medium and the lacquer, if such a suitable material exists, because it is more economical to utilize a single material than to utilize two different materials.

10. **Regarding claims 11, 18, and 25**, Hirose discloses substantially the same invention as the Applicant, except for the through-holes being 20 micrometers in diameter.

11. At the time the invention was made, it would have been an obvious matter of engineering design choice to a person of ordinary skill in the art to apply the method of Hirose to through-holes of this size, because Applicant has not disclosed that this particular through-hole size provides an advantage, is used for a particular purpose, or solves a stated problem that would not be provided or solved by any other through hole size. The through-hole size depends on the particular design of the circuit, and applying the method of APA and Hirose to through-holes of say a 140 micron diameter is as obvious as applying the method to a hole with a 20 micron diameter and vice versa, since the process steps are identical, irrespective of the hole diameter.

12. **Claims 9, 10, 12, 16, 17, 19, and 23, and 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose in view of APA (Applicant's admitted prior art).

13. Hirose discloses substantially the same invention as the Applicant, except for the strip conductors being carbon, individual circuit boards being separated by milling, and the insulating lacquer being an International Standard Organization lacquer.

14. APA teaches that it is known to form carbon circuit patterns (step 8, page 5), to separate individual circuit boards by means of a milling process (step 10, page 5), as well as to use an ISO insulating lacquer (step 7, page 4) in manufacturing printed circuit boards.

15. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to apply these concepts in making the circuit board of Hirose, for the same advantages as when used in the prior art of APA.

Response to Arguments

16. Applicant's arguments filed 8/6/2008 have been fully considered but they are not persuasive.

17. Applicant argues Hirose forms layers 38 and 42, thereby introducing additional layers between the steps of etching and applying the insulating lacquer.

18. The examiner respectfully disagrees. Layer 38 (Fig. 1D) is not an actual layer, it is merely layer 34 having a roughened surface. See step 2 in col. 15. A chemical treatment is used, which coarsens the surface of conductor layer 34. Layer 42 can be a separate layer formed by electroless plating, but Hirose discloses (see ln. 67 of col. 15 to ln. 5 of col. 16) that a coarsened layer can also be formed by a chemical process. In other words, just as with layer 38, layer 42 can actually be nothing more than a roughened surface of conductor layer 34 of Fig. 2F. Therefore, no actual new layers are applied.

19. Regarding the rejection of claims 6-12 under 35 U.S.C. 103(a), these arguments are moot, in view of the new grounds of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LIVIUS R. CAZAN whose telephone number is (571)272-8032. The examiner can normally be reached on M-T 6:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Vo can be reached on (571)272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. Dexter Tugbang/
Primary Examiner
Art Unit 3729

/L. R. C./ 9/29/2008
Examiner, Art Unit 3729